The Motorola Raster Memory System

Making professional graphics affordable for the next generation of graphics systems

MOTOROLA INC.

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LOW COST GRAPHICS FOR:

- *Personal Computers*
- *Work Stations*
- *Videotex Terminals*
- *Computer-Animated Graphics*
- *Word Processing*

WITH THESE FEATURES:

- *Multiple-processor Compatibility*
- *Multimode Operation*
- *32-Color Selectivity (From a Universe of 4096 Shades)*
- *Virtual Screen Accommodation*
- *Smooth Scrolling*
- *Memory Expandability*

2-CHIP SYSTEM

Today's electronics technology permits the generation of CRT-displayed graphics with all the fidelity of a first-quality color motion picture; but not at a price that is compatible with that of low and medium-priced micro-computerized equipment. Today, high quality graphics generation requires several printed circuit boards, densely packed with SSI/MSI integrated circuits, at a cost substantially above what is tolerable for microcomputers...even for some of the more sophisticated minis. Therefore, the overwhelming majority of graphics displays—for both business and entertainment—still suffer from the limited resolution and color selectivity associated with relatively crude arcade games.

But a significant breakthrough is in the offing. Using VLSI processing, Motorola has reduced the multi-board chip complement housing the complex circuitry for high-quality graphics to only two monolithic chips. At an anticipated combined price of less than $20.00 (in production quantities) this chip set portents a major upgrading of low and medium-priced computer graphics.

Though not yet in volume production, the design is sufficiently advanced to permit demonstration,* and to warrant consideration for the next generation of equipment design.

*It has recently been demonstrated at the Consumer Electronics Show, Las Vegas, Nevada, January 5-9, 1984.

MPU CHOICES

The Motorola RMS chip set actually consists of two chips which, under MPU control, convert a graphics program stored in memory to the complex video stream that produces high-quality information on the CRT. This two-chip video display generator set, supplemented by a microprocessor, memory to store the program data, and a small number (as little as three packages) of additional SSI/MSI interface chips, form a complete system. The interface chips act as "glue" for variations in overall hardware architecture.

Eventual display quality is controlled by the processing power of the MPU, the amount of available memory, the quality of the software and, of course, the capabilities of the video display generator. In this regard, the RMS chip set is designed to operate compatibly with three of Motorola's most advanced MPUs: the MC68000, 16/32-bit processor; the MC68008 which has all the processing power of the MC68000, but is designed with 8-bit data lines; the MC6809 with its 16-bit (rather than 32-bit) internal architecture and 8-bit data bus. This compatible MPU complement allows price/performance tradeoffs consistent with end-use requirements.

Going hand-in-hand with MPU selectivity is the ability of RMS to support memory capacity ranging from 16K to 1M Bytes. Again, end-use requirements determine the amount of memory, hence the cost, of the memory needs.

But the breakthrough comes in the myriad of functions crammed into the 2-chip graphics generator to provide the control for high-quality CRT graphics...resulting in a capability so pervasive that graphics quality is primarily dependent on the power of the MPU, the amount of memory available, and the sophistication of the software—*not by any limitations within the RMS system itself.*

- *Internal 96-character ROM*
- *8 reusable true objects*
- *Bit plane or list mode graphics*
- *Broad selection of attributes*
- *Kanji capability*
- *NTSC and PAL compatibility*

MULTI-MODE VIDEO

The RMS provides three unique sources of video generation: Bit plane graphics, list mode graphics, and true objects.

Bit plane displays can contain 4 colors in any resolution, and 16 colors in any horizontal resolution up to 320 pixels. They are most useful for creating complex graphics screens, interactively, under MPU control.

The RMS list mode is a character-oriented mode that supports up to 32 colors and four basic types of characters: alphanumerics, mosaics, fixed objects, and Dynamically Redefinable Characters (DRCs).

The major advantage of the list modes is their attributes. These include flash, double high/double wide characters, inverse video, priority, collision detection and reporting, etc.

True objects are small patterns in memory that the RMS can place on the screen, independent of the object's position in memory, simply by writing to X and Y position registers. The RMS provides eight true objects.

A major strength of the RMS is that the available modes of video operation are independent of the system configuration. Thus a high level of video performance is available over a wide range of system implementations.

CHOICE OF RESOLUTION

RMS operates with most popular CRTs. It will drive monitors with a 50 Hz field refresh rate, used in Europe, or with a 60 Hz rate popular in the U.S. And in either system you have a choice of resolutions up to 640 pixels per line, and up to 500 lines per screen (with 50 Hz refresh). For text reproduction, screen resolutions of either 32, 40, 64, or 80 characters per line are available...in full color. For graphics interpretation, choices of 256, 320, 512, or 640 pixels per line provide the needed definition to fit the application. All these choices are software selectable from internal horizontal and vertical resolution registers.

32 COLOR SELECTIVITY

RMS always operates in a full color mode. It can simultaneously display any 32 colors from its palette of 4096 colors. These are stored in a Color Mapping RAM (CMR) which is addressed, at pixel rate, as the video picture is generated. The system is extremely color selective, permitting the programmer to obtain adjacent pixels only slightly different in shade, as in flesh tones, or completely different in color, as in the reproduction of company logos.

- *Memory image larger than displayed screen*
- *Independent size and width registers to define the virtual screen*

VIRTUAL SCREEN ACCOM-MODATION

The user can construct a Virtual Screen much larger than the monitor's displayed screen using the RMS, then change the visible area by scrolling. The Virtual Screen can occupy as much as ½ Mbyte of memory, giving as much as:

15 displayed screens of 4-color bit plane (640 W x 210 H)

15 displayed screens of 16-color bit plane (320 W x 210 H)

174 displayed screens of 80-character x 25-character listmode (these will vary with the displayed screen's resolution)

The virtual screen can be almost any rectangle as large or larger than the displayed screen, varying in steps as small as one pixel or character row vertically, and 8 pixels or 2 characters horizontally. Three registers define the virtual screen's size, width, and start address.

- *Horizontal and Vertical Scroll*
- *Single Pixel Scrolling Resolution*
- *Minimal MPU Involvement*
- *Barrel Scroll or Edge Mask Effect*
- *Separate Position Registers for Objects*

SMOOTH SCROLLING

The RMS creates that perception of realistic screen motion by providing smooth scrolling in both the horizontal and vertical directions. The visible screen displayed in either bit plane or list mode can be moved within the larger virtual screen by one or more pixels at a time. This capability acknowledges the importance of processing time by requiring a minimum of actual MPU involvement. Since the hardware needed to display an image is controlled by only a few position registers, the entire background can be offset by a single line and/or pixel, or changed completely, in a matter of microseconds. Once the displayed screen is scrolled to the edge of the virtual screen, the programmer can select one of two boundary conditions: a barrel scroll (simply wrapping around to the opposite end of the virtual screen), or a single color edge mask that borders the virtual screen. Although controlled by a separate set of position registers, true objects can also be moved, pixel by pixel, providing lifelike animation.

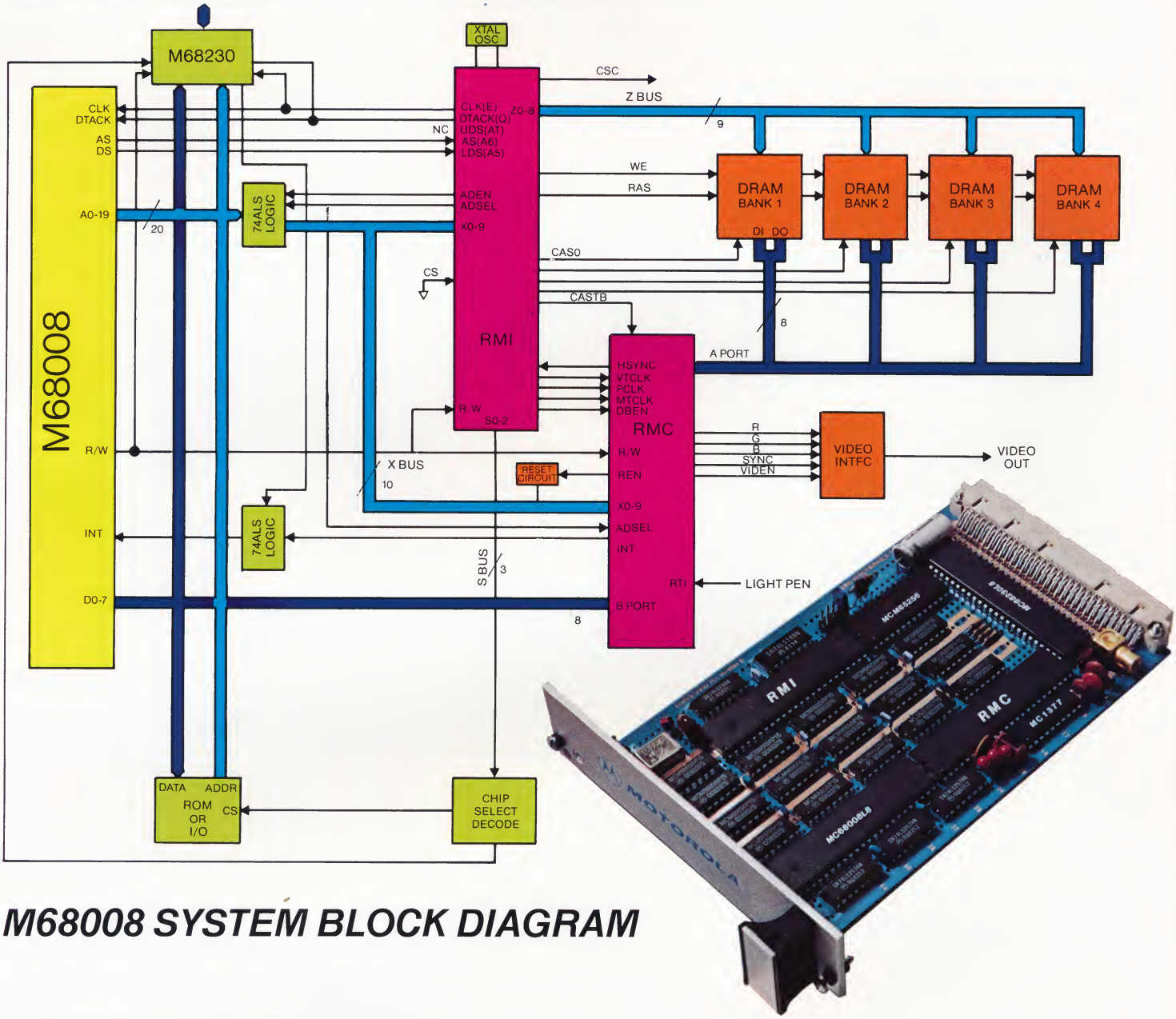
- *Supports 16KX1, 64KX1, 16KX4, and 256KX1 DRAMs*
- *Memory is shared by MPU and Display*
- *All memory timing, refresh, and buffering supported by RMS*
- *Supports 16K to 1M byte of DRAM directly*

MEMORY EXPANDABILITY

To provide maximum flexibility in system implementation, the RMS chip set operates in conjunction with dynamic RAM configurations from as small as 16K bytes to as large as 1M byte. It interfaces directly with several industry standard DRAMs; specifically, 16KX1, 64KX1, 16KX4, and 256KX1. Since memory is shared between the RMS and the MPU, the system designer need only concern himself with how much memory he would like; the RMS will take care of all the timing and refresh requirements. To minimize the total system RAM size, the MPU can access the shared dynamic RAM at the same time that it is being used for display purposes.

As little as one bank of memory is required to support the RMS system, but as system evolution or enhanced performance dictates, two or even four banks (equal length—byte-wide blocks) of memory can be configured to support higher level processors or more complex graphics. In general, the flexibility, expandability, and simplicity of memory interface to the RMS chip set is among its most significant features.

One Board Does It All



M68008 SYSTEM BLOCK DIAGRAM

RMS System The MPU-based System is quite straightforward and uses primarily VLSI devices. The major elements are the desired MPU, the RMS chip set, one to four banks of dynamic RAM, some "glue" and a video interface part. Additional RAM and I/O parts can be easily attached. The RMS itself consists of two parts: the Raster Memory Interface (RMI) and the Raster Memory Controller (RMC).

The RMI is a bipolar digital part built in Motorola's MOSAIC 1.5 process. This process provides the performance of Advanced Low-power Schottky (ALS) logic and also supplies the technology needed for high-density bipolar components. RMI provides the clock generation required for the entire system: the RMS, the MPU, and most peripherals. In addition, it provides DRAM timing, and passes address information between the MPU, the RMI and the RMC (via the X bus) as well as control information from the RMC to the RMI.

The RMC The RMC is a VLSI part fabricated in Motorola's HCMOS technology. The RMC uses the X bus to pass display addresses to the RMI. Once the RMI has addressed the DRAM, the data stored in the addressed locations is read by the RMC which, in turn, processes the data into video pixel information. Thus, the RMC is responsible for generating the sequence of memory addresses in which the video data is stored, and for converting this data into the video information passed on to the CRT.

The memory cycle in RMS allows nine chances to pass data on the X bus. Two of these are reserved for MPU address, two more are reserved for display addresses passed from RMC to RMI, and the remaining five cycles are used for control information.

Personal Computer Graphics System Comparisons

The following table compares the characteristics of the Motorola Raster Memory System (RMS) with those generally employed in today's high-, medium-, and low-end personal computer graphics equipment.

ATTRIBUTES	HIGH END	MID RANGE	LOW END	RMS
Resolution	640 x 200	320 x 210	320 x 210	640 x 500
Virtual Screen				✓
Smooth Scroll Horiz.				✓
Smooth Scroll Vert.				✓
Color Palette*	16/16	16/16	16/4	4096/32
Screen Memory (max)	16K	16K	64K	1024K
Processor Memory Space	1024K	64K	64K	16,384K
80 Characters	✓			✓
DRCS**			✓	✓
Kanji				✓
Objects			8	8
No. Of Memory Images			46	256
Color/Object			4	32
Overlay				✓
NAPLPS Videotex	Fair	Fair	Fair	Excellent
Approx. IC Parts Count (in a typical system - less RAM)	130	45	40	14

*Palette: universe of colors available
**DRCS: Dynamically Redefinable Character Set

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"Graphics chip set paints a broad spectrum"

is the headline over the cover story of the January 26 issue of ELECTRONIC DESIGN. The article, featuring the Motorola Raster Memory System, and co-authored by Motorola engineers, is reprinted on the following pages for your information and convenience.

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